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**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**

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Complete if Known

Application Number	10/643,585
Filing Date	August 18, 2003
First Named Inventor	Scott, Steven
Group Art Unit	2186
Examiner Name	Tsai, Sheng

Attorney Docket No: 1376.700US1**US PATENT DOCUMENTS**

Examiner Initial *	USP Document Number	Publication Date	Name of Patentee or Applicant of cited Document	Filing Date If Appropriate
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OTHER DOCUMENTS -- NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
st		"Cray Assembly Language (CAL) for Cray X1™ Systems Reference Manual", Section 2.6, Memory Ordering, http://docs.cray.com/books/S-2314-51/index.html , (June, 2003), 302 pgs.	
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st		ABTS, D., "So Many States, So Little Time: Verifying Memory Coherence in the Cray X1", <u>Parallel and Distributed Processing Symposium</u> , (April 22, 2003), 11-20	
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sat		PATTERSON, D. A., et al., <u>Computer Architecture: A Quantitative Approach</u> , 2nd Edition, Morgan Kaufmann Publishers, Inc., San Francisco, CA, (1996), 699-708	
sat		PATTERSON, D. A., et al., <u>Computer Architecture: A Quantitative Approach</u> , 2nd Edition, Morgan Kaufmann Publishers, Inc., San Francisco, CA, (1996), 179-187, 373-384	
sat		PATTERSON, D. A., et al., <u>Computer Architecture: A Quantitative Approach</u> , 2nd Edition, Morgan Kaufmann Publishers, Inc., San Francisco, CA, (1996), 194-197	

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